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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 25

Application Number: 09/000,626
Filing Date: 12/30/97
Appellant(s): Rengarajan et al.

Stanton C. Braden

For Appellant

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GROUP 2800

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 11-06-00.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

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(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is deficient because the as-filed disclosure only supports an uppermost surface of the nitride liner disposed below a transistor channel depth. There is no support, literal or otherwise, for the claim limitation requiring the uppermost surface of the nitride liner to be disposed "just below" a transistor channel depth, as in claim 1, lines 7-8. It is also important to note that the specification contains no data or comparative examples to show that the problem identified has actually been solved.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejections of claims 1-5, 7 and 24-25 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

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(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

JP 57-159038	Fukuda et al.	01-1982
5,872,045	Lou et al.	02-1999
5,972,778	Hamada	10-1999

S Wolf, Silicon Processing for the VLSI Era, Vol. 2 - Process Integration, pages 45 & 154, 1990

(10) Grounds of Rejection

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-5, 7 and 24-25 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The recitation of "an uppermost surface of said nitride liner being disposed just below a transistor channel depth" can be interpreted as setting forth structure

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not supported by the disclosure. The disclosure only supports the formation of an uppermost surface of the nitride liner below the channel depth.

Claims 2-5, 7 and 25 are necessarily rejected since these claims directly or indirectly depend upon the rejected base claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-5, 7, 24 and 25, insofar as in compliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda (JP 57-159038 of record) in view of Lou et al. (US 5,872,045 of record), Wolf (reference U of record), and Hamada (US 5,972,778).

Fukuda discloses a trench isolation structure (Figs. 4a-4e) comprising a V-shaped trench in a substrate 10; a nitride liner 12' recessed within the trench and the nitride liner forming a partially enclosed volume; an oxide layer 11' formed within the trench, the oxide layer underlying the nitride liner 12'; a polysilicon 5 to fill in the trench; and an oxide layer 11 on the top surface of the substrate. Fukuda does not disclose using a dielectric material of oxide to fill the trench. However, both polysilicon and oxide are materials known in the art and routinely used to fill trench isolation structure. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select any one of these materials as a suitable trench

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fill in Fukuda's device, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416. In fact, Lou et al. discloses the formation of trench isolation structure with an oxide or polysilicon filling the trench (col. 1, lines 35-60). As a result, the modified Fukuda has the oxide fill formed above the nitride liner and no polysilicon material is formed within the trench.

Fukuda does not explicitly disclose the uppermost surface of the nitride liner 12' being disposed below or just below a transistor channel depth of a transistor beside the trench isolation structure. However, it is old and well known in the art that shallow trench isolation structures are formed in the substrate in order to isolate and define an active region that includes a transistor and source/drain regions that define a channel region. Therefore, the incorporation of a transistor in an active region beside the trench isolation structure of Fukuda is prima facie obvious. Also, it is old and well known in the art that shallow trench isolation region is notoriously formed much deeper than source/drain regions in order to effectively isolate active regions that include channel regions defined by source and drain regions, as shown for example by Wolf (a shallow trench isolation structure formed in the substrate about 5000-8000 angstroms deep) (page 45, line 28) and Hamada (channel depth in the range of 200 to 1500 angstroms). As a result, the channel region is formed very shallow near a top surface of a substrate and the trench isolation region is formed with a depth at least 5 times deeper than that of the channel region. The nitride liner is formed only on the bottom portion of the trench as taught by Fukuda; therefore, it is obvious the modified Fukuda's device provides a nitride liner below or just below the transistor channel depth.

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Since appellant has not defined "just below" and how "just below" is different from "below" anywhere in the disclosure so one skilled in the art would understand the distinction between the relative terms "just below" and "below", it would be reasonable for one person skilled in the art to consider the nitride liner of the modified Fukuda formed either below or just below the channel depth.

Regarding claim 2, Fukuda does not specifically disclose a P-FET transistor. It is old and well known in the art to form trench isolation structure in the support circuitry with P-FET transistors generally employed.

Regarding claim 3, Fukuda does not explicitly disclose a nitride liner wherein the uppermost surface is disposed greater than 1000 angstroms below a top surface of the substrate. It would have been obvious to select the depth of the uppermost surface of the nitride liner since it depends on the trench's depth. The trench's depth may vary with specific designs. Trench's depth in semiconductor devices is an art recognized variable of importance which is subject to routine experimentation and optimization. Accordingly, it would be well for one within ordinary skill in the art to select the depth of the uppermost surface of the nitride liner as taught by Fukuda in association with the trench's depth selection. Also, the application contains no disclosure of either the critical nature of the claimed dimension or any unexpected results arising therefrom. In *re Daily*, 93 USPQ 47 (CCPA 1966), the court held that changes in size and shape of parts of an invention in the absence of an unexpected result involves routine skill in the art. Additionally, In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469

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U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. Furthermore, the application provides no indication that this particular chosen dimension is unconventional. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimension is critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ 2d 1934, 1936 (Fed. Cir. 1990). In fact, the combination of Fukuda, Wolf and Hamada clearly discloses a nitride liner wherein the uppermost surface is disposed greater than 1000 angstroms below a top surface of the substrate.

Regarding claims 7 and 25, it is conventional to fill the trench isolation with an oxide fill of TEOS. Therefore, the incorporation of an oxide fill of TEOS into the Fukada's device is prima facie obvious.

The claim limitation "for preventing hot carrier effects due to charge trapping" in the claim preamble of claim 24 specifies an intended use or field of use is treated as nonlimiting since it has been held that in device claims, intended use must result in a structural difference between the claim invention and the prior art in order to patentably distinguish the claim invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). Also, a claim containing a "recitation with respect to the manner in which a claimed apparatus is

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intended to be employed does not differentiate the claimed apparatus from a prior art apparatus” if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

The claim limitation “to prevent hot carrier effects due to charge trapping ... transistor” in claims 1 and 24 is a functional language and is given no patentable weight since it has been held that claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). “Apparatus claims cover what a device is, not what a device does.” Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). A claim containing a “recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus” if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). Furthermore, the modified Fukuda has the claimed structure, the uppermost surface of the nitride liner formed below a transistor channel depth; therefore, it would have been obvious that the claimed property (characteristic) is inherently present in the device. Hot carrier effects due to electrical charge trapped in the silicon nitride liner is prevented because the nitride liner formed below the channel depth.

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(11) *Response to Argument*

Appellant argues that the specification clearly states the nitride liner being formed below the channel depth of a transistor and the claim language "just below" is a subset of "below" of the channel depth. Therefore, one skilled in the art would understand that "below the channel depth" includes "just below the channel depth". The examiner respectfully disagrees with the remark because "just below" has a narrower meaning than "below", within the context of this specification, and the introduction of claim changes which involve narrowing the claims by introducing elements or limitations which are not supported by the original disclosure is a violation of the written description requirement of 35 USC 112, first paragraph. In *Ex parte Ohshiro*, 14 USPQ2d 1750 (Bd. Pat. App. & Inter. 1989). See MPEP 2163.04.

The invention set forth in this specification is supposed to solve a problem alleged to arise when shallow trench isolation structures containing nitride liners are placed close to P-FET channels. Specifically, hot carriers (presumably high energy holes) are supposed to be trapped within the nitride liner. First of all, it does not appear to be any evidence of record to show that this problem actually occurs. There are no graphs or any other data showing current-voltage characteristics of P channel FETs adjacent to trenches having nitride liners. There are no comparative examples showing a difference in function for devices near nitride-lined trenches compared to devices not near nitride-lined trenches. Possibly the Appellant has such data but chose not to disclose it. Or possibly the specification is in the nature of a thought experiment, in which Appellant speculates that nitride-lined trenches might trap hot carriers, and, if this is in fact

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the case, Appellant then assumes that limiting the height of the nitride liner would solve the problem.

Secondly, a more important point is that no data is presented to show any relationship between specific heights of a nitride trench liner and any hot carrier trapping that may be occurring. Even if one assumes that hot carriers are indeed being trapped in the nitride, and that this effect is indeed having a detrimental effect on nearby transistors, and even if one assumes that limiting the height of a nitride liner to some point below the channel depth would diminish or solve the problem of hot carrier trapping, there is still no evidence that a nitride liner disposed "just below" a transistor channel depth would have any effect on hot carrier trapping, or on the functioning of nearby devices. Quite possibly a nitride liner that extends to "just below" the channel depth would still trap hot carriers, because "just below" the channel depth may be close enough to the channel current to allow for high energy carriers to pass into the nitride. Quite possibly, a nitride liner that extends to "just below" the channel depth would not solve or measurably diminish the effects of the problem identified. So, while "just below" is in some grammatical sense a subset of "below", there is no evidence of record to show that liner heights meeting this limitation would actually solve the problem identified by the specification. Therefore, the addition of the claim limitation of "disposed just below a transistor channel depth" as a description of the height of a nitride trench liner is new matter, because there is no literal support in the specification for the phrase "just below", and because one cannot imply this limitation from the limited nature of the teachings actually included in the specification.

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In response to appellant's argument in subsection C of page 7 of the appeal brief that the combination of Fukuda, Lou, Wolf and Hamada fails to teach an uppermost surface of a nitride liner being disposed just below a transistor channel depth. Since appellant has not defined "just below" and how it is different from "below" anywhere in the disclosure so one skilled in the art would understand the distinction between "just below" and "below". It would be reasonable to a person having ordinary skill in the art at the time the invention was made to consider the uppermost surface of the nitride liner of the modified Fukuda disposed relatively either below or just below a transistor channel depth.

On page 8 of the appeal brief, appellant also states that the examiner admits Fukuda does not disclose the uppermost surface of the nitride liner disposed below a transistor channel depth. The examiner disagrees with the remark because in the office action the examiner only said "Fukuda does not explicitly disclose the uppermost surface of the nitride liner 12' being disposed below or just below a transistor channel depth of a transistor beside the trench isolation structure" which is different from "does not disclose" as appellant alleged. Besides, appellant argues against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appellant also argues that the mere fact that the prior art could be modified does not make the modification obvious unless the prior art references suggest the desirability of the

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modification. The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969). Besides, Fukuda teaches the principal element of appellant's invention that is a recessed nitride liner on the bottom portion of the trench isolation region with an uppermost surface of the nitride liner inherently disposed below the channel depth of a transistor. Other elements that are not explicitly disclosed by Fukuda are conventional features that are obvious to form for conventional reasons in the vicinity of the trench isolation as discussed above.

In response to appellant's argument on page 9 of the appeal brief that the present invention performs differently from the prior art. The prior art suffers hot carrier effects while the present invention reduces these effects. First, appellant fails to provide any scientific evidence to support appellant's argument that the prior art suffers hot carrier effect and performs differently from the present invention. Second, the combination of Fukuda, Lou, Wolf and Hamada clearly teaches a recessed nitride liner on the bottom portion of the isolation trench wherein the uppermost surface of the nitride liner is below or just below the channel depth of a transistor, therefore, no nitride is formed adjacent the channel region to trap charges and cause hot carrier effects as appellant alleges. Therefore, the combination of Fukuda, Lou, Wolf and Hamada performs the same function that the present invention does.

For the above reasons, it is believed that the rejections should be sustained.

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Respectfully submitted,

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